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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,454	03/15/2004	Jim Sweet	15562US02	1218

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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,454	SWEET, JIM	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Figure 2B, item 205 as disclosed in paragraph 35. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Paragraph 36, line 9 references item number 216 as a multiple-input AND gate. Examiner recommends replacing with 218 as shown in drawing 2C.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al.

With regard to claim 1, Davis et al. teach a method for sharing hardware resources in a digital system, the method comprising:

Determining whether a hardware resource (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor) is in use by monitoring contents of at least one of a plurality of semaphore registers (Figure 4 shows the process of a thread attempting to lock a resource. In the case where the thread wins arbitration, but finds the semaphore already locked, it may return back to the round robin selection (start, item 100, item 110, item 120, item 130, item 150, item 170).

Examiner interprets this as the thread monitoring the contents of semaphore registers "Sem_Val" and "Sem_Lock").

Davis et al. fail to teach accessing said monitored contents of said pluralit y of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

Baker et al. teach a limited-width test bus whose bus width contains less than a number of bits needed to individually address all of the address space (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 2, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

With regard to claim 11, Davis et al. teach the additional limitation of a method according to claim 1 further comprising determining from said monitored contents of said plurality of semaphore registers an identifier of a software thread using said hardware resource (paragraph 25).

With regard to claim 12, Davis et al. teach the additional limitation of a method according to claim 11, further comprising tracking said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claims 13 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Ando et al.

With regard to claim 13, Davis et al. teach a plurality of semaphore registers (paragraph 25; Figure 3), but fail to teach arranging the registers into register blocks, and selecting one of said plurality of semaphore register blocks to be accessed by a limited-width test bus.

Baker et al. teach a limited-width test bus ((column 2, lines 59 – 63).

Ando et al. teach arranging a plurality of registers into register blocks (Figure 1, items 20_1 to 20_4), and selecting one of said plurality of registers to be accessed by a bus (bus: Figure 1, item 1; selection: column 4, lines 9 – 12, 17 – 26; column 6, lines 6 – 9, 17 – 20)

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to organize the semaphore registers as taught by Davis et al. into register blocks as taught by Ando et al. This would have been obvious in order to simplify the decoding circuit and reduce the number of signal lines required to access the registers (column 7, lines 9 – 24).

With regard to claim 14, Baker et al. teach the additional limitation of assigning at least one bit line in the bus to select one of said plurality of semaphore register blocks (where a memory device may be interpreted as a register block; column 3, lines 24 – 27).

With regard to claim 15, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

* * *

Claims 19, 20, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al.

With regard to claim 19, Davis et al. teach a system for sharing hardware resources in a digital system, the system comprising:

A plurality of hardware resources (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor – Examiner interprets these as hardware resources);

A plurality of semaphore registers coupled to said plurality of hardware resources (paragraph 21 describes a semaphore being mapped to a memory, data store, embedded processor);

Davis et al. fail to teach a limited-width test bus coupled to said plurality of semaphore registers, wherein said limited-width test bus contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

Baker et al. teach a limited-width test bus whose bus width contains less than a number of bits needed to individually address all of the address space (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 20, Baker et al. teach the additional limitation of assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers (where a semaphore register may be interpreted as a memory device; column 3, lines 11 – 14, 24 – 27) and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers (column 3, lines 11 – 14, 43 – 47).

With regard to claim 27, Davis et al. teach the additional limitation of a system according to claim 19, wherein a processor coupled to said limited-width test bus (where a processor may be interpreted as a semaphore coprocessor; paragraph 18) determines an identifier of a software thread that is using one of said hardware

resources based on contents of at least one of said plurality of semaphore registers (where an identifier may be interpreted as a thread ID; paragraph 25).

With regard to claim 28, Davis et al. teach the additional limitation of a method according to claim 27, wherein said processor tracks said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claims 29 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. in view of Baker et al., and further in view of Ando et al.

With regard to claim 29, Davis et al. teach a plurality of semaphore registers, but fail to teach the registers organized in blocks, a selector coupled to said plurality of semaphore register blocks, and a limited-width test bus connected to said plurality of semaphore registers blocks of said selector.

Ando et al. teach a plurality of register blocks comprising a plurality of registers (Figure 1, items 20_1 to 20_4), and a selector coupled to said plurality of semaphore register blocks (where a selector may be interpreted as a decoder; Figure 1, item 27; column 4, lines 9 – 12, 17 – 26; column 6, lines 6 – 9, 17 – 20).

Baker et al. teach a limited-width test bus (column 2, lines 59 – 63).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to organize the semaphore registers as taught by Davis et al. into register blocks as taught by Ando et al. This would have been obvious in order to simplify the decoding circuit and reduce the number of signal lines required to access the registers (column 7, lines 9 – 24).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the limited-width test bus as taught by Baker et al. into the method of Davis et al. for the purpose of reducing the number of pins needed for the bus. This would have been obvious since Baker et al. teach that reducing the number of pins required for the bus would reduce the cost of the system and increase the reliability (column 1, lines 23 – 45).

With regard to claim 30, Baker et al. teach the additional limitation of assigning at least one bit line in the bus to select one of said plurality of semaphore register blocks (where a memory device may be interpreted as a register block; column 3, lines 24 – 27).

With regard to claim 31, Davis et al. teach the additional limitation wherein a processor (where a processor may be interpreted as a semaphore coprocessor; paragraph 18) determines whether a hardware resource is in use in said selected one of said plurality of semaphore register blocks (paragraphs 23, 25).

With regard to claim 32, Davis et al. teach the additional limitation of a system further comprising determining from said monitored contents of said plurality of semaphore registers an identifier of a software thread using said hardware resource (paragraph 25).

With regard to claim 33, Davis et al. teach the additional limitation of a system, further comprising tracking said software thread that is using said hardware resource (paragraph 25; Examiner interprets storing the thread identifier in a semaphore register as tracking the software thread, i.e., maintaining knowledge of what hardware resources it is using).

* * *

Claims 3, 5, 6, 8 – 10, 16 – 18, and 20 – 26 are rejected under official notice. Examiner takes official notice that the use of OR/AND/XOR gates is old, and well known in this art for the purposes of determining if all of a number of bits are set to logic 1, logic 0, or if all bits are different, in a digital system.

With regard to claim 4, Davis et al. teach the additional limitation where if a result of a determination is logic 1, then a hardware resource is in use, and if a result of a determination is logic 0, then a hardware resource is not in use (where a result

determination may be interpreted as the value of the Semaphore_Lock register; paragraph 23).

Claim 7 is rejected under official notice. Examiner takes official notice that taking the complement of the values used to determine whether or not a resource is in use as recited in claim 4 would have been well known to one of ordinary skill in this art at the time of invention by applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

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SUPERVISORY PATENT EXAMINER
1/19/06